74. (Amended) A semiconductor device, comprising:

a substrate including an interconnect pattern formed thereover and a protective layer covering said interconnect pattern, said substrate having a first region on which a semiconductor chip is mounted and a second region which surrounds said first region, said protective layer having an edge portion in said second region;

said semiconductor chip including electrodes electrically connected to said interconnect pattern; and

an adhesive between said substrate and said semiconductor chip, the adhesive covering said edge portion, said first region and a part of said interconnect pattern below said edge portion, wherein portions of the interconnect pattern connected to the electrodes of the semiconductor chip remain substantially flat.

REMARKS

Claims 30-85 are pending. By this Amendment, claims 30, 50, 68 and 74 are amended to recite "wherein portions of the interconnect pattern connected to the electrodes of the semiconductor chip remain substantially flat." These amendments are supported by the specification at, for example, Fig. 2B. Thus, no new matter is added. Reconsideration based on the above amendments and the remarks below is respectfully requested.

The attached Appendix includes marked-up copies of each rewritten claim (37 C.F.R. §1.121(c)(1)(ii)).

The Office Action rejects claims 68-71, 73-77, 79 and 82-85 under 35 U.S.C. §102(e) over U.S. Patent 6,208,525 to Imasu et al. This rejection is respectfully traversed.

The Office Action asserts that Imasu discloses all elements recited in claims 68 and 74. However, Applicant respectfully submits that Imasu does not disclose or suggest that an edge of said semiconductor chip does not overlap with said protective layer, ... wherein

portions of the interconnect pattern connected to the electrodes of the semiconductor chip remain substantially flat, as recited in claims 68 and 74.

Imasu discloses a semiconductor chip 10 mounted on a substrate 1 with an adhesive layer 16 therebetween. See Figs. 2 and 11. The semiconductor chip 10 is connected to wiring 4A via bump electrode 15. See col. 5, lines 10-26. The wiring 4A has recesses 4B. See Figs. 2 and 11 and col. 5, lines 36-43.

Imasu discloses a passivation film 5 that is between the semiconductor chip 10 and the substrate 1. See Fig. 2 and col. 4, lines 42-45. The bump electrode 15 has a stud bump structure with a height that is significantly larger than the thickness of the passivation film 5. See Fig. 2; col. 5, lines 27-35; and col. 6, lines 17-20. Thus, even with the existence of the recesses 4B, the height of the bump electrode 15 allows for the passivation film 15 to exist between the semiconductor chip 10 and the substrate 1. See Fig. 2.

Imasu discloses that, when the bump electrode has a ball shape, the passivation film 15 does not exist between the semiconductor chip 10 and the substrate 1. See Fig. 11 and col. 8, 22-27. That is, although the height of the ball-shaped bump electrode is larger than the thickness of the passivation film 5, because a portion of the ball-shaped bump electrode is in the recesses 4B, the clearance between the semiconductor chip 10 and the substrate 1 is reduced such that the passivation film 15 can no longer exist between the semiconductor chip 10 and the substrate 1. See Fig. 11.

In view of the above, Imasu does not disclose or suggest that an edge of said semiconductor chip does not overlap with said protective layer, ... wherein portions of the interconnect pattern connected to the electrodes of the semiconductor chip remain substantially flat, as recited in claims 68 and 74. Thus, Imasu does not disclose or suggest the subject matter recited in claims 68 and 74, and claims 69-71, 73, 75-77, 79 and 82-85

depending therefrom. Withdrawal of the rejection of claims 68-71, 73-77, 79 and 82-85 under 35 U.S.C. §102(e) is respectfully requested.

The Office Action rejects claims 72 and 78 under 35 U.S.C. §103(a) over Imasu in view of Japanese Patent JP356050546A to Shigeki. This rejection is respectfully traversed.

The Office Action admits that Imasu does not disclose or suggest shading, but asserts that Shigeki discloses such a feature. However, Applicant respectfully submits that Imasu and Shigeki, individually or in combination, do not disclose or suggest that an edge of said semiconductor chip does not overlap with said protective layer, ... wherein portions of the interconnect pattern connected to the electrodes of the semiconductor chip remain substantially flat, as recited in claims 68 and 74.

Shigeki merely discloses a semiconductor element with black pigment. See Abstract. Nowhere does Shigeki disclose or suggest that an edge of said semiconductor chip does not overlap with said protective layer, ... wherein portions of the interconnect pattern connected to the electrodes of the semiconductor chip remain substantially flat, as recited in claims 68 and 74. Therefore, Shigeki does not supply the subject matter lacking in Imasu.

For at least the above reasons, Imasu and Shigeki, individually or in combination, do not disclose or suggest to the subject matter recited in claims 68 and 74, and claims 72 and 78 depending therefrom. Withdrawal of the rejection of claims 72 and 78 under 35 U.S.C. §103(a) is respectfully requested.

The Office Action rejects claims 30-67, 80 and 81 under 35 U.S.C. §103(a) over Imasu and Shigeki in view of U.S. Patent 5,918,113 to Higashi et al. This rejection is respectfully traversed.

The Office Action asserts that the combination of Imasu and Shigeki discloses all the limitation of the product as claimed and the method steps are inherent and obvious, if not identical, in view of the product claims. However, Applicant respectfully submits that

Imasu, Shigeki and Higashi, individually or in combination, do not disclose or suggest that an edge of said semiconductor chip does not overlap with said protective layer, ... wherein portions of the interconnect pattern connected to the electrodes of the semiconductor chip remain substantially flat, as recited in claims 30 and 50.

As discussed above, Imasu discloses non-overlapping between the semiconductor chip 10 and the passivation film 5 only under the prerequisite that the wiring 4A has recesses 4B. Thus, Imasu does not disclose or suggest that an edge of said semiconductor chip does not overlap with said protective layer, ... wherein portions of the interconnect pattern connected to the electrodes of the semiconductor chip remain substantially flat, as recited in claims 30 and 50.

As discussed above, Shigeki merely discloses using pigment. Shigeki does not disclose or suggest that an edge of said semiconductor chip does not overlap with said protective layer, ... wherein portions of the interconnect pattern connected to the electrodes of the semiconductor chip remain substantially flat. Therefore, Shigeki does not supply the subject matter lacking in Imasu.

Higashi discloses a process for producing a semiconductor device using anisotropic conductive adhesive. See col. 1, lines 7-10 and col. 3, lines 23-27. Higashi does not disclose or suggest a protective layer. Thus, Higashi does not disclose or suggest that an edge of said semiconductor chip does not overlap with said protective layer, ... wherein portions of the interconnect pattern connected to the electrodes of the semiconductor chip remain substantially flat. Therefore, Higashi does not supply the subject matter lacking in Imasu and Shigeki.

For at least the above reasons, Imasu, Shigeki and Higashi, individually or in combination, do not disclose or suggest the subject matter recited in claims 30 and 50, and

claims 31-49, 51-67, 80 and 81 depending therefrom. Withdrawal of the rejection of claims 30-67, 80 and 81 under 35 U.S.C. §103(a) is respectfully requested.

The Office Action rejects claims 30-85 under the judicially created doctrine of double patenting over claims 1-29 of U.S. Patent No. 6,462,284. A Terminal Disclaimer is concurrently filed in compliance with 37 C.F.R §1.321(c). Accordingly, withdrawal of this rejection of claims 30-85 is respectfully requested.

In view of the foregoing amendments and remarks, Applicant submits that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 30-85 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Gang Luo
Registration No. 50,559

JAO:GXL/ale

Attachments:
Petition for Extension of Time
Appendix
Terminal Disclaimer

Date: May 6, 2003

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

APPENDIX

Changes to Claims:

The following is a marked-up version of the amended claims:

30. (Amended) A method of manufacturing a semiconductor device, comprising:

mounting a semiconductor chip on a substrate, said semiconductor chip having electrodes, said substrate having an interconnect pattern formed thereof and a protective layer covering at least a part of said interconnect pattern, said semiconductor chip mounted on said substrate such that an edge of said semiconductor chip does not overlap with said protective layer;

electrically connecting said electrodes to said interconnect pattern; and

adhering said semiconductor chip to said substrate by an adhesive, said adhesive provided on said substrate from a region in which said semiconductor chip is mounted to said protective layer, wherein portions of the interconnect pattern connected to the electrodes of the semiconductor chip remain substantially flat.

50. (Amended) A method of manufacturing a semiconductor chip, comprising:

providing an adhesive over a substrate which includes an interconnect pattern formed thereover and a protective layer covering said interconnect pattern, said substrate having a first region on which a semiconductor ship is mounted and a second region which surrounds said first region, said protective layer having and edge portion on said interconnect pattern in said second region, said edge portion, said first region and a part of said interconnect pattern below said edge portion covered with said adhesive; and

providing said semiconductor chip including electrodes onto said first region to electrically connect said electrodes to said interconnect pattern, wherein portions of the interconnect pattern connected to the electrodes of the semiconductor chip remain substantially flat.

68. (Amended) A semiconductor device, comprising:

a substrate, said substrate having an interconnect pattern formed thereover, said substrate having a protective layer covering at least a part of said interconnect pattern;

a semiconductor chip, said semiconductor chip having electrodes, said electrodes electrically connected to said interconnect pattern, said semiconductor chip mounted on said substrate such that an edge of said semiconductor chip does not overlap with said protective layer; and

an adhesive, said adhesive adhering said semiconductor chip to said substrate, said adhesive provided on said substrate from a region in which said semiconductor chip is mounted to said protective layer, wherein portions of the interconnect pattern connected to the electrodes of the semiconductor chip remain substantially flat.

74. (Amended) A semiconductor device, comprising:

a substrate including an interconnect pattern formed thereover and a protective layer covering said interconnect pattern, said substrate having a first region on which a semiconductor chip is mounted and a second region which surrounds said first region, said protective layer having an edge portion in said second region;

said semiconductor chip including electrodes electrically connected to said interconnect pattern; and

an adhesive between said substrate and said semiconductor chip, the adhesive covering said edge portion, said first region and a part of said interconnect pattern below said edge portion, wherein portions of the interconnect pattern connected to the electrodes of the semiconductor chip remain substantially flat.